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COMPLIMENTARY METAL OXIDE SEMICONDUCTOR (CMOS)-MEMRISTOR HYBRID NANOELECTRONICS

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14. ABSTRACT

The goal of this project was to explore CMOS-memristor hybrid nanoelectronic circuits for memory, FPGA, DSP, analog, and neuromorphic applications. The specific tasks of the project included: material selection, integration flow development, circuit design and simulation, and development of demonstration vehicle fabrication and testing. The major accomplishments of this effort were, 1) a Verilog-A model of a memristor and co-simulation with SPICE for one transistor one memristor (1T1R) circuits/memory cell, and a memristor-FPGA routing switch were developed; 2) electrical measurements were performed on a memristor-FPGA routing switch demonstration platform, which were compared with simulation results; and 3) an integration strategy for fabricating CMOS/memristor hybrid devices was explored. These results lay the groundwork for follow-on programs that would develop integrated CMOS/memristor devices for the above applications.

15. SUBJECT TERMS
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1. Summary:

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2. Introduction:

Heralded in the December 2008 issue of IEEE Spectrum as "discovery of the year," the memristor is the fourth fundamental passive electronic device in addition to the familiar resistor, capacitor and inductor. By integrating with CMOS devices, memristors show promise for development of revolutionary new nanoelectronic computing architectures with significantly reduced size and extremely low consumed power. The proposed effort explores a novel, high-payoff, nanotechnology area that exploits crossbar nanoelectronic logic elements as well as the recently demonstrated phenomena of memristance [1]. Specifically, the goal of this project was to explore CMOS-memristor hybrid nanoelectronic circuits for memory, FPGA, DSP, analog, and neuromorphic applications.

Crossbar computer logic architectures are complex matrices of interconnected nodes that show great promise for scalability, size, weight and power issues. In their simplest form, crossbar junctions consist of two nanowires (less than 100nm wide) that physically "cross" each other. The junction between these nanowires is composed of a junction material with tailored transport properties. Crossbar logic elements enable massively parallel computations with the potential for a reduction in power consumption and size by up to 2-3 orders of magnitude. Crossbar computing is also tolerant to hardware defects, due to its intrinsic, network-on-chip flexibility to re-route around defects [2]. Preliminary efforts in crossbar computing have been demonstrated by researchers at Hewlett-Packard Laboratories, in which memristive elements were used [3].

In order to take advantage of these quintessential new memristive properties, it is necessary that memristive nanoelectronics be successfully integrated with current CMOS process technology [3-8]. The electronic transport properties of memristive nanoelectronics driven by CMOS circuits will provide critical insights into subcircuit designs and subsequent advanced architectures.

3. Methods, Assumptions and Procedures:

The specific tasks of the project included: material selection, integration flow development, circuit design and simulation, and demonstration vehicle fabrication / testing. Materials selection and integration flow development was performed in conjunction with the CNSE Center for Semiconductor Research. Fabrication engineers were consulted for compatible back end of the line (BEOL) materials with memristive properties and vertical integration design built off of previous work at CNSE for CMOS transistor fabrication. This effort was concurrent with another AFRL sponsored project for development of crossbar memristor devices.

Modeling and simulation were performed using commercially available software including Verilog-A and SPICE. Novel code was written to simulate one transistor/one memristor (1T1R) devices, as well as an FPGA routing circuit utilizing memristive elements. Memristor electrical behavior was modeled as bipolar switching, based on measurements of individual memristive devices within the PI's research group. All other device characteristics were taken from standard CMOS devices using a standard 65nm device platform (IBM proprietary device design package and data).

FPGA/memristor demonstration devices were fabricated by manually connecting individual memristors with transistors using wire bonding, to achieve an FPGA routing switch that could potentially replace an SRAM-based routing switch. This "bread-board" device was then tested in an Agilent 1500 probe station with associated analysis hardware/software.

4. Results and Discussion:

4.1 Key Accomplishments:

During this 6-month project, we finished the following tasks:

- Design and simulation of 1T1R memory
- Design, simulation and measurement of CMOS-memristor FPGA routing component
- Material selection and integration flow suitable for CMOS-memristor integration

4.2 Development of Verilog-A model / SPICE for 1T1R

In this project, we finished the design and simulation of 1T1R structures. We developed the Verilog A model for memristor for Spice simulation. Therefore, we can use SPICE-Verilog A simulator to analyze the performance of a CMOS-memristor 1T1R cells for memory applications. Figure 1 illustrates the simulation result for a 1T1R structure.

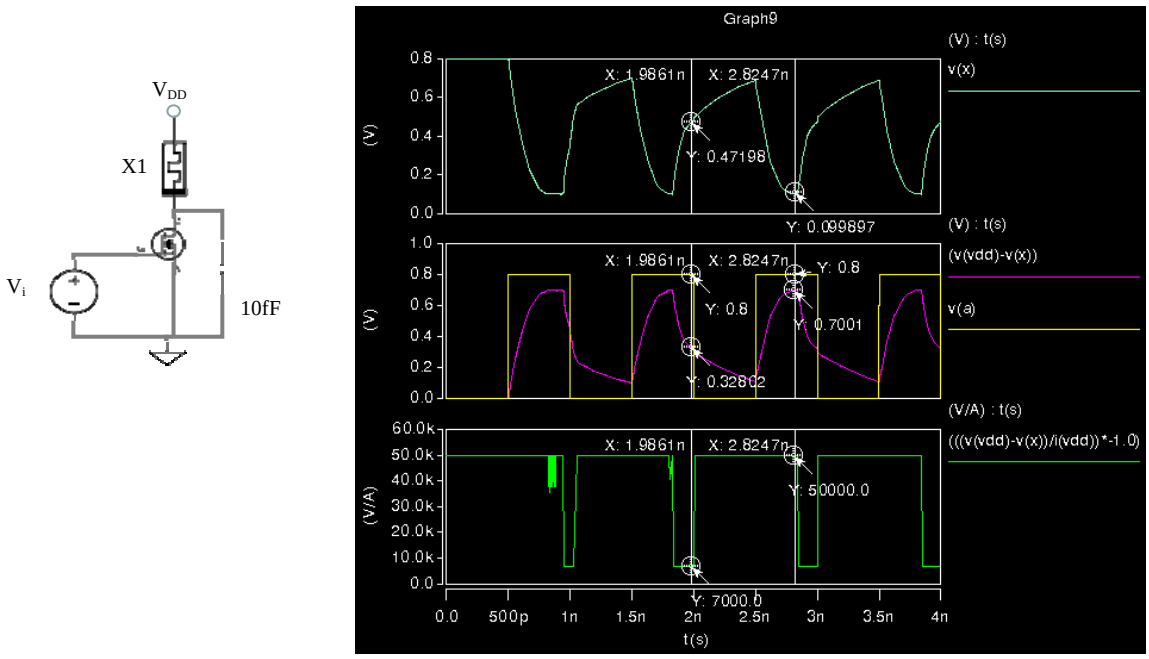

Figure 1. Design and simulation of 1T1R structure.

4.3 Simulation and Measurement for Memristor-FPGA Routing Switch

The second result obtained in this work was the design and simulation of the novel CMOS-memristor routing element. This structure can utilize two complementary memristors to control a pass transistor, providing an efficient routing element for FPGA applications. By using the similar Spice-Verilog A simulation approach, we obtained simulation results (Figure 2). The important comparison was carried out between the simulation and the measurement of the real CMOS-memristor circuitry. The simulation was highly consistent with the measurement, which demonstrates the first measured and simulated CMOS-memristor hybrid routing circuit, to our knowledge.

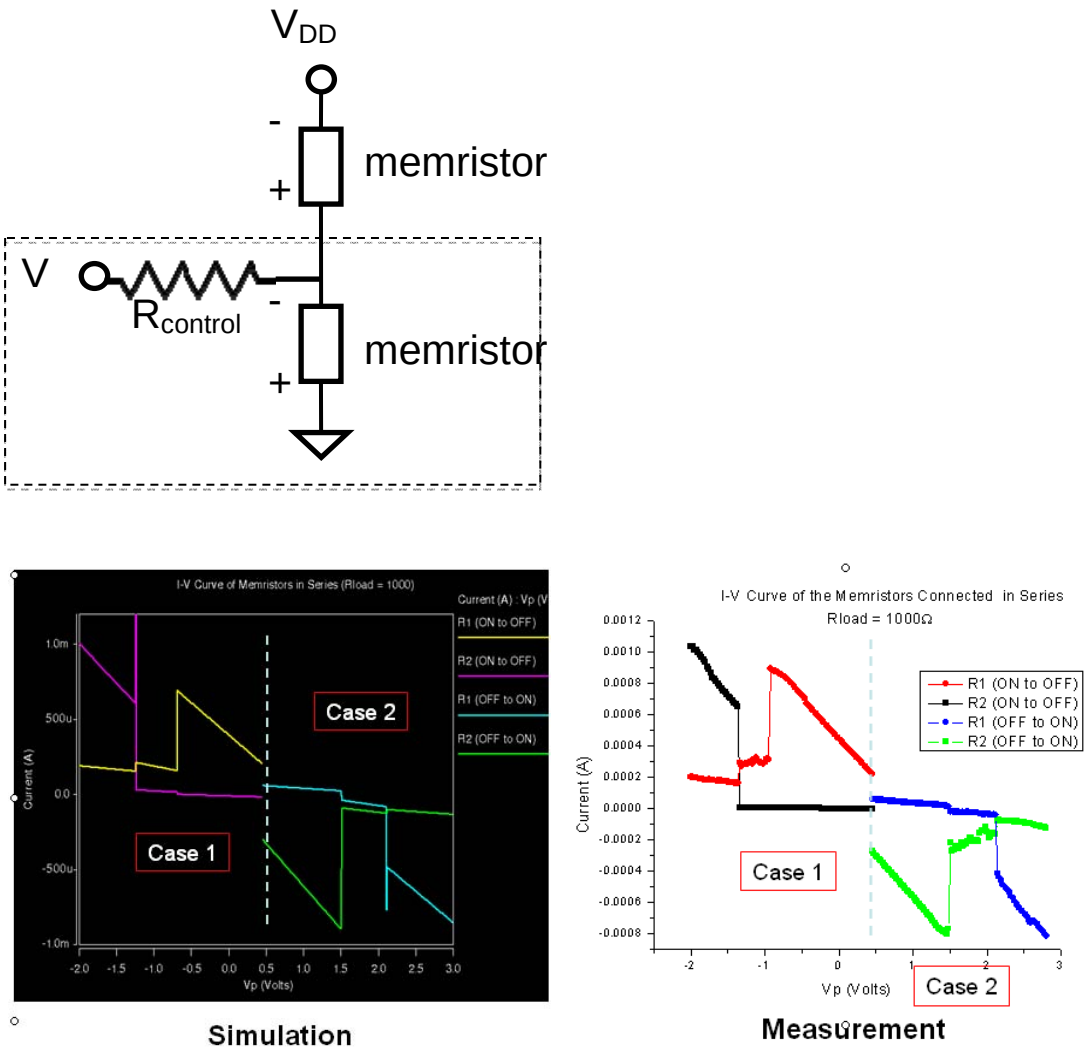

Figure 2. Design and simulation of CMOS-memristor hybrid routing structure.

4.4 Development of Integration Strategy for Fabricating CMOS/memristor Hybrid Devices

In parallel with ongoing memristor development efforts at CNSE, we developed a strategy for fabricating vertically integrated CMOS/memristor hybrid devices. Our materials selection effort focused on oxidation of copper to produce copper oxide memristive structures which could be easily integrated with the copper via/stud back end of the line (BEOL) processing currently used in the CNSE 300mm foundry (Figure 3). The memristive elements can be integrated with source, drain, or gate regions of buried CMOS transistors. Follow-on efforts will focus on demonstration of these hybrid structures and electrical measurement to demonstate their utility in the simulated/modeled 1T1R and FPGA-based structures from this effort.

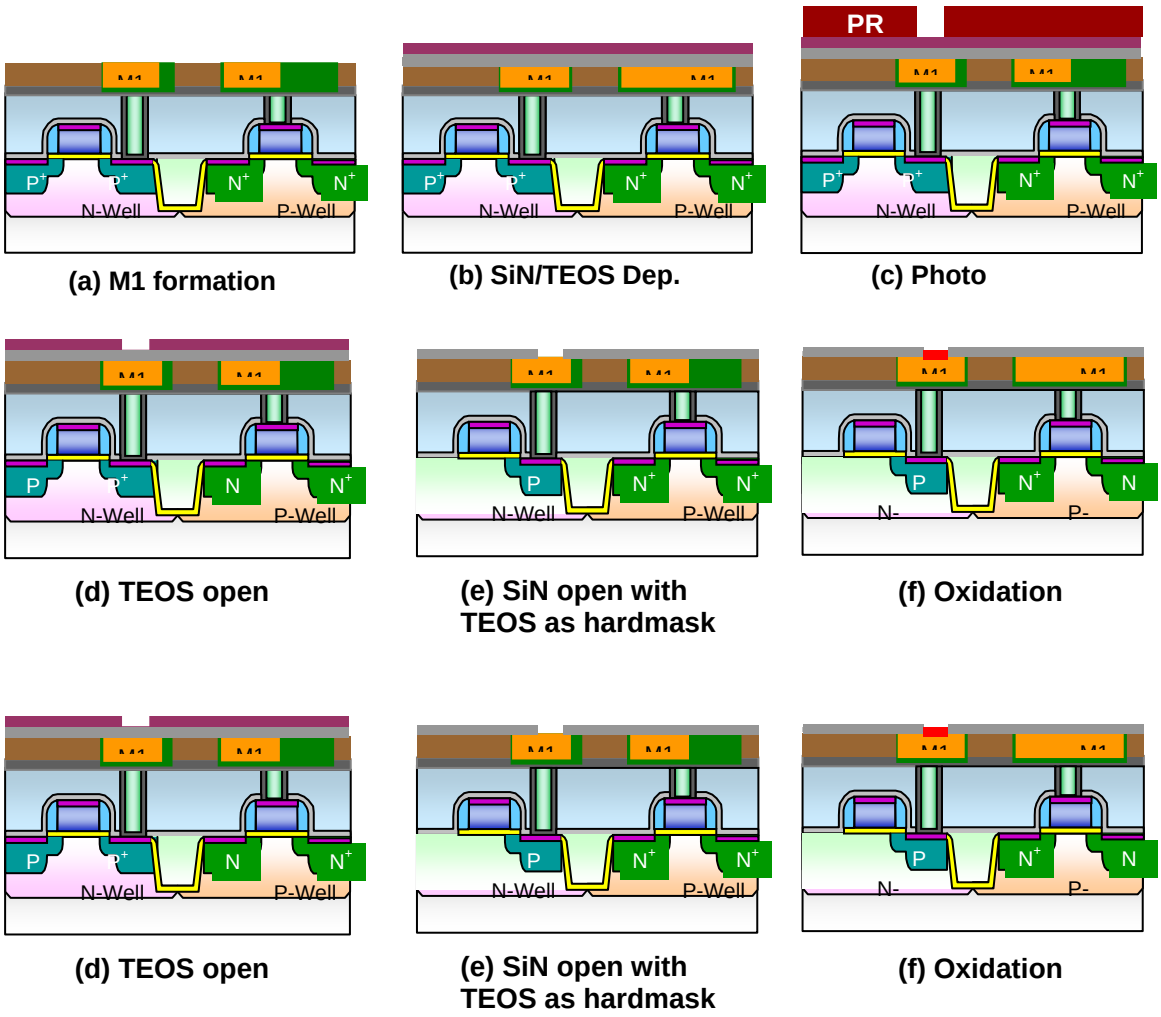

Figure 3. CMOS-memristor integration flow.

4.5 Publications in This Project Period

- W. Wang, Tom T. Jing and B. Butcher, "FPGA based on integration of memristors and CMOS devices", ISCAS 2010, Paris, France, May 2010 (invited paper).
- Ming Liu, Z. Abid, and Wei Wang, "3D Integration of CMOL structures for FPGA applications," IEEE Trans. on Computers, 2010.
- S. Tanachutiwat, Ming Liu, and Wei Wang, "FPGA Based on integration of CMOS and RRAM," IEEE Trans. on VLSI, 2010.
- B. Butcher, X. He, M. Huang, Y. Wang, Q. Liu, H. Lv, M. Liu, and Wei Wang, “Proton-based Total-Dose Irradiation Effects on Cu/HfO2:Cu/Pt ReRAM devices”, IOP Nanotechnology, to appear.

5. Conclusions:

This effort successfully produced simulation data and code for hybrid CMOS/memristor devices. The Verilog-A and SPICE code can be used for future efforts, which could include incorporation of empirical data from device measurements. This will be critical for modeling behavior of integrated CMOS/memristor devices and ensuring that functional devices can be fabricated. This code could also be used for future design work, to inform the design of much more complex circuits. The preliminary measurement data from the FPGA-routing/memristor circuits is also informative for future designs to simplify FPGA routing by incorporation of memristor elements. Finally, the materials selection and process flow development for vertically integrated CMOS/memristor devices lays the groundwork for our follow-on efforts to fabricate these devices.

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7. List of Acronyms:

1T1R: One transistor, one memristor/Re-RAM element

BEOL: Back end of the line

CMOS: Complimentary metal oxide semiconductor

CNSE: College of Nanoscale Science and Engineering

FPGA: Field programmable gate array

TEOS: Tetraethylorthosilicate (silicon dioxide precursor)